ATARI®

SM194

Technical Manual

Februari 1991

TABLE OF CONTENTS

1.0 SCOPE

This document describes a monitor series that covers a range of horizontal scan frequencies and includes options to satisfy requirements in a wide variety of applications.

2.0 GENERAL DESCRIPTION

The monitor series is supplied with a 20-inch diagonal tube with a 114 degree deflection. (15", 17" and 24" CRT's are available.)

The monitor can be custom configured for any horizontal scan frequency from 32 KHz to 128 KHz, and for vertical field frequencies from 49 Hz to 120 Hz.

The specific values included in this document are for a typical monitor operating at a 66 KHz horizontal scan rate. Other scan rate information can be obtained by consulting OEM sales or application engineering.

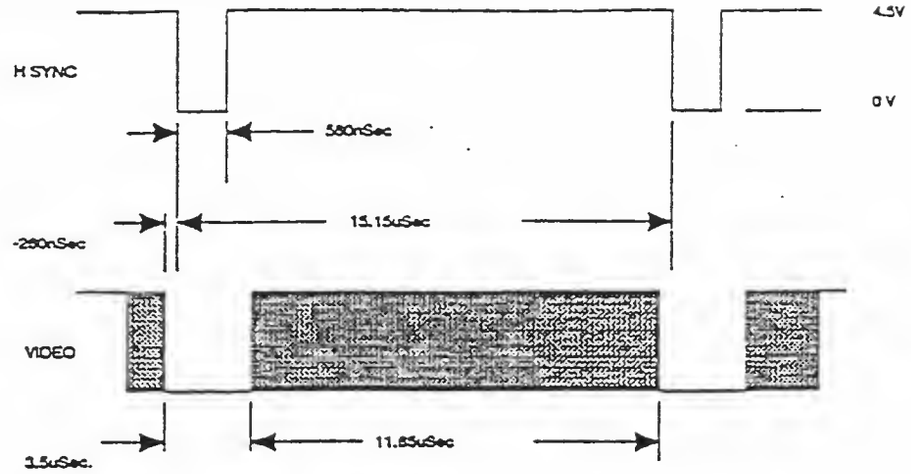
3.0 ELECTRICAL CHARACTERISTICS

3.1 Power Supply:

Input Voltage	90 to 137 VAC or 180 to 264 VAC
Power Frequency	47-63 Hz
Power	64 Watts
Inrush Current	40 Amps peak at 120 VAC 60 Amps peak at 220 VAC

3.2 Input Signals:

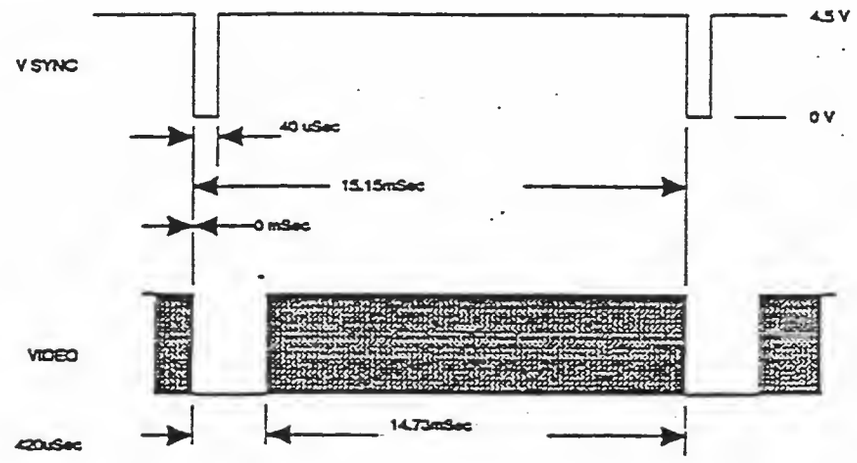
TYPICAL: Horizontal Timing



3.2.1 Horizontal Sync:

Polarity	Negative, edge (Positive Optional)
Signal Level	TTL
Signal rise/fall	TTL
Pulse Width	0.5uSec (min) to 50% of total horizontal scan time
Input Impedance	typical 100 Ohms
Frequency	32 KHz to 128 KHz
Blanking	3.0uSec (min)

TYPICAL: Vertical Timing



3.2.2 Vertical Sync:

Polarity	Negative edge (Positive Optional)
Signal Level	TTL
Signal Rise/Fall	TTL
Pulse Width	40-400 uSec
Input Impedance	typical 100 Ohms
Frequency	49 Hz to 120 Hz (Interlace Optional)
Blanking	450 uSec(min)

3.2.3 Video Signal Input Requirements

Polarity	Positive is white (Negative Optional)
Signal	1 Bit ECL Differential
Input Impedance	Typical 75 or 100 Ohms

4.0 DISPLAY PERFORMANCE

4.1 Input Conditions:

Character	"@"
Brightness	At raster cutoff
Contrast	White level input video should be set to result in 30 Foot-Lamberts in P4 or equivalent setting.
Viewing Direction	Along the CRT neck axis
Viewing Distance	18 inches
Ambient Temp.	25 degrees C
Supply Voltage	120 VAC
Warm up time	20 minutes max.
Display size	14 x 11 inches +/- 0.1"

4.2 Video:

Rise/Fall times	3.5 nSec Max. (10% - 90%)

4.3 Horizontal:

Video blanking	3.0 uSec Horizontal(Min.)
Horizontal Scan Delay	0-4 uSec Adjustable Phase Control

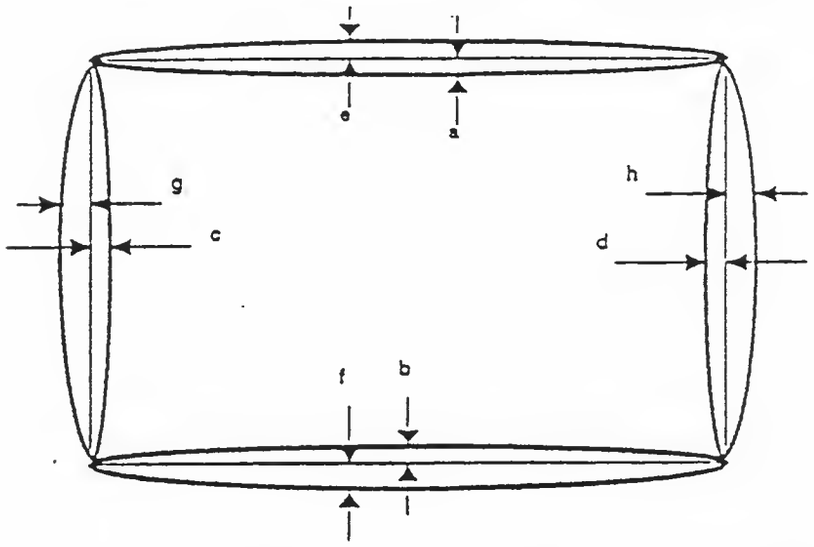
4.4 Vertical:

Video blanking	450 uSec Vertical (Min.)

4.5 Image Distortion:

4.5.1 PINCUSHION AND BARREL:

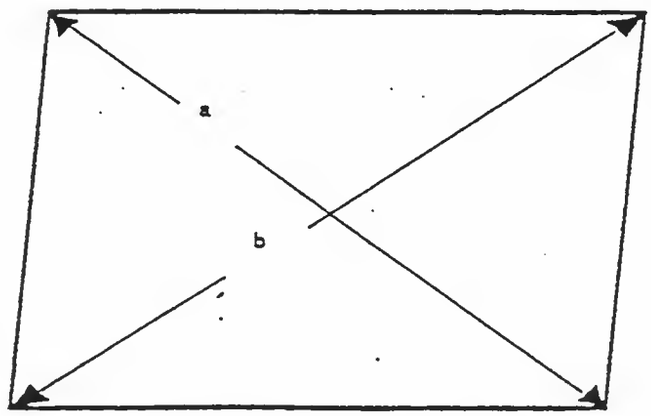
Input Image A rectangle outlining the video perimeter



Pincushion or Barrel: a through h
0.07" max
Incremental Pincushion: 0.085" max within 2"
0.045" max within 1"

4.5.2 Parallelogram:

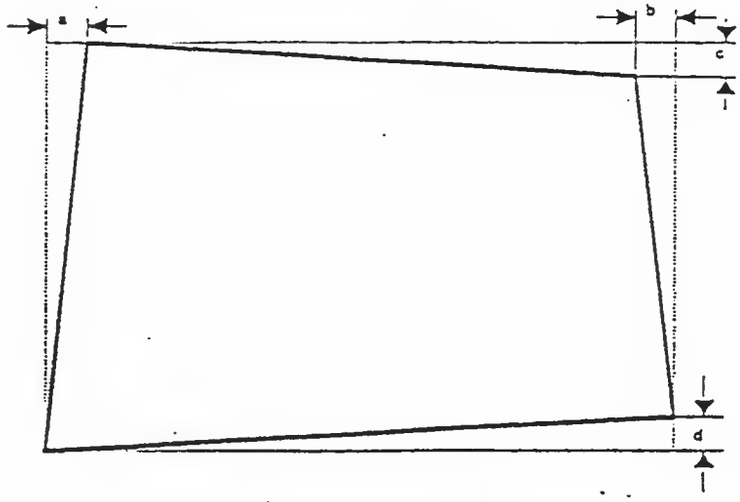
Input image A rectangle outlining the video perimeter



Diagonals (a , b) are within 2%

4.5.3 Trapezoid:

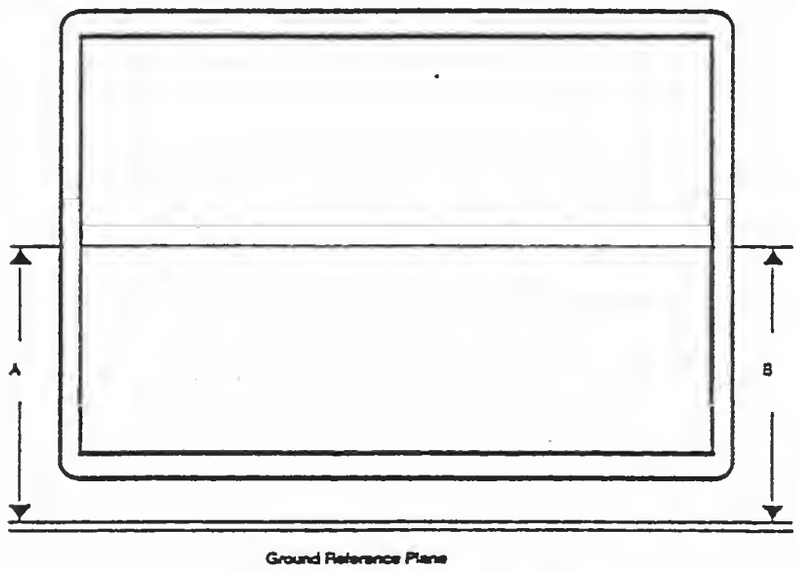
Input image — a rectangle outlining the video perimeter



Distances a through d 0.14 inches max

4.5.4 Rotation:

Input image — a rectangle outlining the video perimeter.

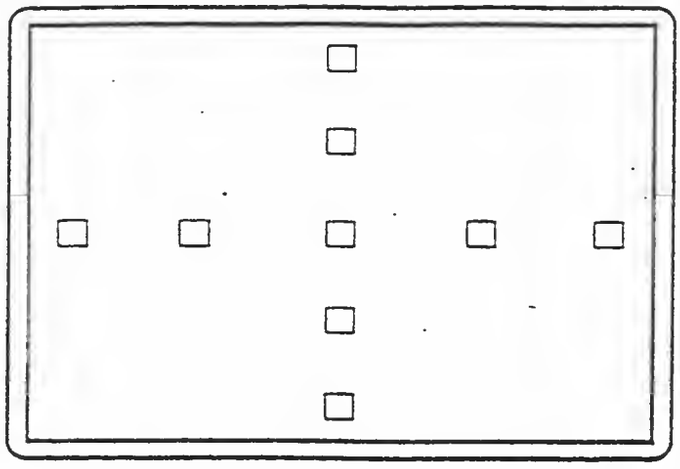


A – B = 0.07 inches max

4.5.5 Center Bow:

0.07 inches max

4.5.6 Linearity:



Using the above pattern, the linearity shall be better than 7% vertically and better that 9% horizontally.

4.6 Resolution: 1300 Lines min. at 10 Ft-L
P104 phosphor and standard 48%
Transmission glass

4.7 Light Output: 30 Ft-L min. with max settings

4.8 Display Stability:

4.8.1 Jitter:

Jitter and Swim resulting from Monitor Generated Sources: Radiated power line interference of 0.005 inch max., down to a frequency of 47 Hz.

Interference from other nonsynchronous sources shall not produce more than 0.003 inches of jitter on the display.

4.8.2 Turn on Drift:

After a 10 minute warm-up, the periphery of the display shall not drift more than 0.10 inches in any direction. During the 10 minute warm-up, the display shall not "wrap around" the raster.

4.8.3 High Voltage Regulation:

With an all white active display, dimensions shall not change by more than 0.5%, when going from 2 Ft-L to 30 Ft-L light output (ref. P104 phosphor).

4.8.4 Black Level Stability:

When changing the data pattern from 5% Average Picture Level (APL) to 100% APL, the reference black level will stay constant with 2%.

5.0 CONTROLS

5.1 User:

Brightness
Power Switch
Contrast (Available on Grey Scale Units)

5.2 Internal:

Contrast
Brightness
Horizontal Centering (Phase)
Horizontal Size
Horizontal Linearity
Vertical Size
Vertical Linearity
G2 Bias
Static Focus
Vertical Dynamic Focus
Horizontal Dynamic Focus

6.0 OPTIONS

6.1 Video:

TTL 1 to 3 Bits
ECL 1 to 3 Bits
Analog Composite Video, RS343A

6.2 Phosphors:

P104 standard
All phosphors available as options

6.3 Anti-Reflection Treatment:

Fine Etch or Polished is standard
Bonded quarter wavelength optical coated panel available as options

6.4 Orientation Format:

Landscape and portrait with horizontal scan in Long or Short dimension

6.5 Controls:

Remote contrast
LED Power indicator

6.6 Power:

ECL Supply: -10.0VDC nominal @ 500 ma

7.0 MECHANICAL DESCRIPTION OF OPTIONAL CABINET WITH TILT-SWIVEL BASE:

Overall Height	14.5"	(368mm)
Overall Width	17.8"	(452mm)
Overall Depth	15.0"	(381mm)
Rear Panel Dimensions	13.0 x 9.5"	(330 x 241mm)
Weight	36 Lbs.	(16.4 Kilograms)

8.0 ENVIRONMENTAL PERFORMANCE

Operating Temperature (in box)	5 to 55 degrees C
Storage Temperature	-40 to 65 degrees C
Humidity	5% to 95% noncondensing
Operating Altitude	10,000 Ft. max.
Nonoperating Altitude	40,000 Ft. max.

Vibration:

Sweep 5-500-5Hz: 0.5g max from 0 to 200 Hz, 0.33g max from 200 to 500 Hz. Duration of sweep is 15 minutes; then 15 minute dwell on peak resonant at 0.55g.

Shock:

20g vertically, longitudinally and laterally, half-sine wave with pulse width 11-15mSec.

9.0 AGENCY COMPLIANCE

The unit is designed to meet the following requirements:

UL478 Fourth Edition Listed/Recognized

CSA C22.2 No. 154

IEC 380, VDE 0806 GS Mark, and VDE 0871 Class B in cabinet

DHHS 21 CFR, Subchapter J, X-Ray Certified

FCC Class B, Part 15 in cabinet

10.0 INTERFACE

AC Power In: CEE-22 Receptacle or AC Safety Interlock

10.1 Input Signals:

Connector: 9 Pin Subminiature D

Typical Pin Assignments

	ECL	TTL
1.	ECL Video	TTL Video
2.	ECL Video Return (GND)	N/C
3.	H Sync	H Sync
4.	V Sync	V Sync
5.	N/C	N/C
6.	ECL (Not) Video	TTL Video Return (GND)
7.	ECL (Not) Video Return (GND)	H Sync Return (GND)
8.	Sync Return (GND)	V Sync Return (GND)
9.	N/C	N/C

NOTE: Other Pin Assignments readily accommodated.

10.2 Analog Input:

Analog Input: BNC - RS343A Levels

11.0 THEORY OF OPERATION

11.1 Deflection Board

The deflection board does several tasks;

i) processes sync
ii) provides horizontal yoke deflection
iii) provides vertical yoke deflection
iv) provides a sync pulse to the power supply
v) provides the required focus voltage
vi) provides spot burn protection

i. Sync Processing

The 74LS221 U4 is a dual non-retriggerable one shot with Schmitt trigger inputs. Noise is reduced by the hysteresis in the inputs and the non-retriggered action. Jumper blocks JR1/JR2 are provided to select the active edge.

The TLC555 U1 is a level triggered timing device used in the same mode as U4.

The leading edge of horizontal sync triggers the one shot U4. The end of time out triggers the TLC555 U1. The second delay is needed to delay the signal a full line. The end of time out of U1 triggers Q1 for a duration determined by C18 and R12. The PLL then centers this pulse on flyback. The data centering potentiometer V10, should be set to center the video in the raster. The amount and range of delay is set by R37, R68 and V10.

Vertical sync is fed through the one shot U1 to get better noise immunity, to offer the option of inversion and to allow some delay for interlace requirements.

ii. Horizontal Deflection

The phase locked loop is used to synchronize the horizontal switch to the timing pulses from the computer or signal generator.

The delayed sync from U1 is buffered through Q1 with its pulse width set (by R12 and C18) and is capacitively coupled to the PLL, U2. The sync is fed into pin 3 of the MC1391. This sync pulse determines when U2 (MC1391/PLL) samples the ramp waveform generated by the yoke and available to pin 4 of U2. The ramp waveform is capacitively coupled to U2. If the sampling occurs at different positions on the ramp at pin 4, an error voltage is generated at pin 5. The error voltage is connected to pin 7

through a low pass filter. Pin 7 is the timing input of U2, therefore the error voltage created by the phase or frequency difference between the flyback and sync signals controls the oscillator. See figure 1 for waveform details.

The free run frequency of U2 is determined by V1, R19 and C7. The duty cycle of U2 is determined by R16 and R17. The output is pin 1 which determines the drive of the FET Q3. The FET Q3 is normally on until U2 pulls the gate low and shuts off Q3.

The switching of Q3 drives the horizontal output transistor Q7 through a current transformer. When Q3 is turned on, Q7 turns off. The Baker's clamp D23 is an optional component.

On the right hand half of the screen, transistor Q7 is conducting current through the deflection yoke to ground. This current is provided by the "S" correction capacitor(s) C25 (C44), which has a charge approximately equal to the supply voltage. The damper diode D10 allows current to flow from ground through the deflection yoke to C25 giving the left hand half of the screen.

The flyback capacitor(s) C24 (C43), connects the hot side of the yoke to ground. This component determines the size and length of the flyback pulse.

The "S" shaping capacitor(s) C25 (C44) is used to correct linearity since the CRT face has a larger radius of curvature than does the deflecting electron beam. The capacitor(s) corrects the outside versus center of screen linearity. There is a DC voltage equal to the supply voltage plus a parabolic voltage with a peak to peak value of 35 to 90 volts depending on the setup. If the value of C25 is reduced this parabola will increase, reducing the size of the outside characters with respect to the center characters.

Left versus right linearity is controlled with the linearity coil L2. This is a saturable coil in the path of the yoke current. Like the size coil, any inductance in series with the yoke will reduce the size of the picture. This saturable coil will change inductance with amplitude and direction of current flow through it. In this case at the start of a trace the linearity coil has an inductance of 20% of the yoke. By the center of the trace, the linearity coil inductance has decreased to about 5% of the yoke where it remains for the rest of the trace. This variable inductor should be adjusted so the right and left sides of the picture are the same size.

Horizontal centering is done with the dual variable coil L1. These two variable inductors are in one unit and are connected from the supply voltage to the cold side of the yoke. In conjunction with D11 and D12 one inductor is connected for the right half of a trace and the other serves the left half. If the two inductors are equal (when the slug is in the center, or removed completely), then the average current flow is zero and the picture is not shifted. If there is an imbalance in inductance then there will be a net flow causing the picture (raster included) to shift position on the screen.

iii. Vertical Deflection

The TDA1670 incorporates all the necessary functions for providing the yoke with the current required for vertical deflection. Incorporated in silicon is a synchronizable oscillator, ramp generator, voltage regulator, voltage doubler and power amplifier.

The oscillator is an integrator (pins 4 to 3) and a two threshold comparator which switches pin 6 high or low to allow the charging of C8. D3 allows the charge and discharge ramps to have adjustable slopes. Vertical sync pulses come in on pin 5. See figure 2.

The ramp generator is made up of a current generator, controlled by current through pin 7, and the capacitor C12 from pin 9 to ground. The slope and thus the size of the linear ramp is adjustable by setting the current pulled from pin 7 through V3. This ramp also appears buffered on pin 10 at a much lower impedance.

The power amplifier, with input on pin 12, sums the ramp on pin 10 with the current ramp through the yoke. R31 and C14 stabilize the high gain power amplifier. Yoke current flows from pin 1, through the yoke, the DC blocking capacitor C16, and the current sampling resistor R33 to ground. Voltage which represents yoke current is then fed back to the input of the amplifier to be compared with the reference.

The output stage of the power amplifier is supplied by the 25 volt supply during the trace, and by the flyback generator circuit during the retrace. The internal clock turns off the lower output stage to start flyback. The power output stage is thermally protected by sensing the junction temperature and shutting off the current source of the power stage.

The DC bias point is maintained by the divider R34, R32 and R33. Capacitors C16 and C15 find the average output voltage. This voltage is then fed back into the input of the buffer amplifier where it is compared to a reference. Any difference in these two voltages causes the DC bias point of the power amplifier to self-adjust.

In order to obtain sufficiently short flyback times, a voltage greater than that required during scan must be applied to the yoke. The flyback generator, during flyback only, supplies (to the power amplifier) a voltage equal to double the supply voltage. Pin 15 charges a capacitor C9, up to the supply voltage during trace and then sets this capacitor on top of the power supply during retrace, thus doubling the available voltage.

Vertical linearity adjustments interact with size adjustments. The ramp from pin 10 is subtracted from the ramp across R33 and the results are fed back to the size input, pin 7 of the TDA1670.

Vertical "S" shaping is done by using the TL431 (U9) and C21 with R38 as an integrator. The vertical ramp across R33 integrated becomes the vertical parabola on the output of U9. This parabola is fed back to the vertical size input, pin 7 of the TDA1670 and compensates for "S" distortion. The parabola is also used to drive the vertical focus modulator. Diode D6, resistors R38, R39, R40 and capacitor C17 develop a bias voltage.

Vertical centering is accomplished with a current source or sink. If V5 is adjusted so that it is a current sink, then the picture (raster included) will move up the screen. If V5 is adjusted so that it provides current, then the picture will move down the screen. Potentiometer V5 should be set to center the data, not the raster , on the screen.

iv. Power Supply Sync

The power supply is synchronous with the horizontal deflection in order to reduce the switching noise. This is accomplished by sending a stepped down version of the horizontal flyback pulse by sampling the pulse on the blocking inductor T2.

v. Focus Modulation

Each section of the CRT screen focuses at a different voltage. The center of the screen may require several

Horizontal centering is done with the dual variable coil L1. These two variable inductors are in one unit and are connected from the supply voltage to the cold side of the yoke. In conjunction with D11 and D12 one inductor is connected for the right half of a trace and the other serves the left half. If the two inductors are equal (when the slug is in the center, or removed completely), then the average current flow is zero and the picture is not shifted. If there is an imbalance in inductance then there will be a net flow causing the picture (raster included) to shift position on the screen.

iii. Vertical Deflection

The TDA1670 incorporates all the necessary functions for providing the yoke with the current required for vertical deflection. Incorporated in silicon is a synchronizable oscillator, ramp generator, voltage regulator, voltage doubler and power amplifier.

The oscillator is an integrator (pins 4 to 3) and a two threshold comparator which switches pin 6 high or low to allow the charging of C8. D3 allows the charge and discharge ramps to have adjustable slopes. Vertical sync pulses come in on pin 5. See figure 2.

The ramp generator is made up of a current generator, controlled by current through pin 7, and the capacitor C12 from pin 9 to ground. The slope and thus the size of the linear ramp is adjustable by setting the current pulled from pin 7 through V3. This ramp also appears buffered on pin 10 at a much lower impedance.

The power amplifier, with input on pin 12, sums the ramp on pin 10 with the current ramp through the yoke. R31 and C14 stabilize the high gain power amplifier. Yoke current flows from pin 1, through the yoke, the DC blocking capacitor C16, and the current sampling resistor R33 to ground. Voltage which represents yoke current is then fed back to the input of the amplifier to be compared with the reference.

The output stage of the power amplifier is supplied by the 25 volt supply during the trace, and by the flyback generator circuit during the retrace. The internal clock turns off the lower output stage to start flyback. The power output stage is thermally protected by sensing the junction temperature and shutting off the current source of the power stage.

hundred volts less than the top or bottom of the screen, while the left and right require more.

To achieve the best focus over all, the focus voltage is modulated with both a vertical and horizontal signals. The vertical parabola developed at U9 drives the emitter of the common base configured Q5 which is a high voltage amplifier. The collector of Q5 then has a high voltage parabola of vertical frequency.

The horizontal focus parabola is developed from the voltage on "S" capacitor C25. The parabola developed from the yoke deflection current at C25 is stepped up through T3 and added to the vertical parabola at Q5 to provide the focus voltage.

The autotransformer T3, is a multitapped transformer to accommodate different "S" capacitor waveforms and CRTs. The focus potentiometer V6, sets the DC focus voltage.

vi. High Voltage Shut Down/Spotburn Protection

If the deflection circuitry, horizontal or vertical, stops functioning at required frequencies, the high voltage supply will be shut down. If Q9 does not receive a signal at the horizontal rate, C39 will charge up and turn Q10 on which will provide a positive voltage to the remote shut down pin on the power supply causing the high voltage to shut down. Likewise, if Q8 does not receive a signal at the vertical rate C38 will charge up and turn on Q10 resulting in high voltage shut down.

11.2 Power Supply

11.2.1 Low Voltage Supply

The design utilizes a discontinuous flyback topology operating in current-mode resulting in a multiple output switcher with outputs which track well. Small or no output filter chokes are needed and slower diodes can be used. The fast transient response of the control loop maintains picture integrity. Very fast current limiting protects the switcher against short circuit.

The input rectifier section converts the AC line voltage into a crudely filtered and unregulated DC voltage, which powers the switching regulator. The input section is configured as a fullwave bridge when operated from 220V line, and as a voltage doubler when operating from 110V. There is a header available to select either mode of operation.

To reduce noise transmission to and from the power line, a low pass filter isolates the switcher. The conducted noise is reduced by X and Y capacitors and a common mode transformer.

3842 (U1), is an integrated current mode pulse width modulator. It consists of an oscillator, error amplifier, current sense comparator, under-voltage lockout and an output MOSFET driver stage. The under-voltage lockout circuit insures that Vcc is adequate to make the 3842 fully operational before enabling the oscillator, voltage reference or output stage. Turn-on turn-off are fixed internally at 16V and 10V respectively. The 6V hysteresis prevents Vcc oscillations during power sequencing.

The oscillator consists of a pull up resistor R11, from the 5V reference to pin 4 and a timing capacitor to ground. When the voltage ramps up to 2.8V on pin 4, an internal current sink pulls down, discharging the timing capacitor to a 1.0V level. This level releases the current sink and starts the next cycle. The free running oscillator frequency is approximately equal to 1/.55RC.

3842 can also be synchronized to an external clock. This is achieved by capacitively coupling a stepped down signal of the horizontal flyback pulse through C33 to the timing capacitor C10. Noise immunity is enhanced if the free running frequency of the oscillator is set to be about 20% less than the clock frequency.

The output stage of the 3842 has a single totem-pole output capable of operating to 1A peaks and a 200 mA average current.

3842 utilizes a current sense comparator. Current mode controllers inherently keep close watch over the pass transistor's current Q1. Pin 3 is connected to a voltage comparator which shuts off the output when the current in the primary winding of the power transformer reaches the desired level, as prescribed by the error amplifier. This way the controller will only allow the needed amount of power to be stored in the output transformer.

Current mode control differs from most pulse width controllers which compare the error amplifier's output against the oscillator's voltage ramp. This results in control of on-time, which does not necessarily mirror the power stored in the transformer.

The current sense comparator also serves the dual purpose of monitoring current limit. If pin 3 rises above 1V the output is terminated. Therefore, output short-circuits and core saturations should be detected before destroying Q1.

The error amplifier of the 3842 has the inverting input on pin 2, non-inverting input tied to an internal 2.5 V reference and an output on pin 1. The voltage on pin 2 is compared to the 2.5V. Errors in output voltage are amplified and fed to pin 1 where they are frequency compensated by an RC back to pin 2. This error voltage is internally dropped by 1.4V and divided by 3 before being fed to the current comparator. At the current comparator, the error amplifier output sets the level at which the current sensed at pin 3 will ramp up to, thereby setting the amount of energy stored in the power transformer and therefore, the power at the output.

In this application, an operational amplifier U4, located on the secondary side of the switcher, compares a single output voltage to a regulated reference voltage. Any error in output voltage is amplified by U4. The output is frequency compensated by R24 and C24. Error current is fed through the optocoupler to the error amplifier of the 3842.

3842 draws very little current in start-up mode. There is enough power from the line bleeders R2 and R3 to slowly charge C8 to the 16V needed to start the switcher. When switching begins, Vcc falls quickly but before it reaches the 10V shut-off level the auxiliary winding on the power transformer provides the required power.

As the 3842 starts a cycle, it turns on transistor Q1. This allows current to flow in the primary of T1. As current ramps up with time, the voltage across the current sense resistor R7 also ramps to a point where U1 determines enough power has been stored via the comparator, and turns off Q1. As the voltage on Q1 flies upward, power is dumped from the main power transformer T1 through diodes into the different outputs. Primary ringing which could over voltage Q1, is clamped by D2. Currents from the secondary windings are rectified and filtered to create the desired output voltages.

11.2.2 High Voltage Supply

The high voltage power supply is a resonant mode regulator. The input supply voltage is 25V DC. The 25V input is regulated down to 15V by U3. This regulated 15V is divided down and used as the reference voltage input of the operational amplifier U4. The inverting input is the

feedback from the anode. POT2 adjusts the reference voltage for the non-inverting input and thus the anode voltage. In addition to the anode voltage, 1200V and -120V are developed from the same transformer.

The remote shutdown will shut the high voltage supply down if the voltage at the base of Q5 reaches approximately 6V.

11.3 1BIT ECL Video

The main functions of the 1Bit ECL video board are driving the cathode and arc protection. The rest of the grid voltages are coupled through the ECL board and arc protected, but are not modified by the video board.

The ECL signal is received by U1 through J1-2,3 . R1, R2, R3 and R4 are the termination resistors and D1, D2, D3 and D4 are clamp diodes. The inverted signal goes to pins 2, 6, 10 and 14, and the non-inverted input goes to pins 3, 7, 11 and 15 of U1. U1, MC10H125, is an ECL to TTL translator. The output of the U1 drives Q1, which drives the cathode.

When Q1 turns on, Q2 turns off pulling the cathode low. When Q1 turns off, Q2 turns on pulling the cathode high. L1 is a peaking inductor for the amplifier which helps Q2 turn on and off faster during it's transitions.

Any ripple or other noise on the voltage driving the cathode will probably show on the screen as shading. This makes it necessary to filter the supply voltage, and is done with C11, C12, C7, C8 and L2.

Arc protection is provided for G1, G2, G4 and the cathode. Arc gaps are used for G1, G2 and G4 and a gas arc gap used for the cathode. These gaps provide a short circuit if the voltage across them reaches a certain threshold. One side of the gap is connected to the grid it is protecting, while the other side is connected to the arc return ground. The arc return ground is separate from the signal ground and is connected directly to the CRT dag.

When the anode arcs to an element of the CRT gun, the gap fires creating a short circuit directly back to the CRT dag, thus protecting the circuitry.

11.4 Analog Video, Low Bandwidth

The low bandwidth analog video board has a bandwidth of about 90MHz. It uses the MC10115, (U201 and U202) quad differential amplifier. The general circuit consists of a sync stripper, sync separator, dc restore and video amplifier. The analog board also provides arc protection similar to the 1BIT ECL video board.

The sync stripper consists of Q202, Q203 and their supporting circuitry. This circuits' function is to remove the sync signals and to provide a composite sync signal for further processing.

Some setups require a separate composite sync signal from the video signal. These systems would not require a sync stripper and only need proper termination supplied by R237 and R236. Note that R236 and R237 are optional components, however in case of R236 optional applies to it's value. If composite video is used R236 should be a 1k ohm resistor.

The sync separator separates the vertical sync signal from the composite signal. This is accomplished with an exclusive OR gate, U204A. One input is tied directly to the composite sync and the other to a filtered composite sync. The horizontal rate is filtered out by R234 and C223. The output is a negative vertical sync signal. Composite sync is used for the horizontal sync signal.

The dc restore circuit tells the video amplifier what voltage level represents a black video level. The video voltage level is sampled during blanking and compared to a reference voltage (set by R238) by U203B. The trailing edge of the horizontal sync is used to shut Q204 off. This turns on Q205 and allows a sample of the cathode voltage to reach the operational amplifier U203B. The output of U203B is fed to U202 and U201.

The video amplifier circuit consists of U201, U202, Q207, Q208 and Q209 and their supporting circuitry. U201 and U202 compare the black level set by U203B to the input video signal and amplify the difference. R211 sets the input level and therefore the gain. The outputs of U201 and U202 together act as another differential amplifier, increasing the gain of the circuit. The remote contrast pot sets the current draw through Q207, which sets the swing on the cathode.

Pin 1 of the MC10115 is the collector of the output transistor and pin 2 (3, 14, 15) is the emitter. Tying the emitters together gives the differential amplifier

configuration of U201 and U202. The inverting inputs of U201 are tied to the non-inverting inputs of U202 and visa versa. The larger the difference between black and input video levels, the more U201 turns on (the less U202 turns on), which in turn drives Q207 on, forcing the cathode lower, resulting in a brighter video.

C203, C204 and C205 are peaking capacitors. R211 sets gain or contrast as does the remote contrast potentiometer.

11.5 Analog Video, Medium Bandwidth

The medium bandwidth analog board has a bandwidth of about 135MHz. It's functions are sync signal stripping, sync signal separation, DC restore and video amplification. It also provides arc protection for all circuitry.

The sync stripper consists of U105A, Q103, Q104 and Q105 and their supporting circuitry. The collector of Q105 has the composite sync signal stripped from composite video. Some setups have a separate sync signal from video signal. This is allowed by JR101. Composite video uses JR101-A and separate sync uses JR101-B.

The sync separator separates the vertical sync signal from the composite signal. This is accomplished with an exclusive OR gate, U103D. One input is tied directly to the +5V line and the other to a filtered composite sync. The horizontal rate is filtered out by R132 and C118. The output is a negative vertical sync signal. Composite sync is used for the horizontal sync signal.

The trailing edge of the horizontal sync activates Q106 causing a positive gate signal to pin 5 of U101 for U101 to sample the black level video. U101 is a video preamplifier with internal black level restore and gain control. The output is coupled to Q101 where it is buffered and sent to the video driver amplifier U102.

U102 is an LH2424 video driver amplifier. It operates off a 60V supply. The input on pin 1 is amplified and drives the output, pin 9, which is coupled to the cathode.

R106 controls the DC level or black level. R108 limits the range of the remote contrast potentiometer. JR101 is used to select between separate and composite sync. JR102 is set, so pin 6 on U103 has a negative going sync output. C111 and C112 are peaking capacitors.

APPENDIX

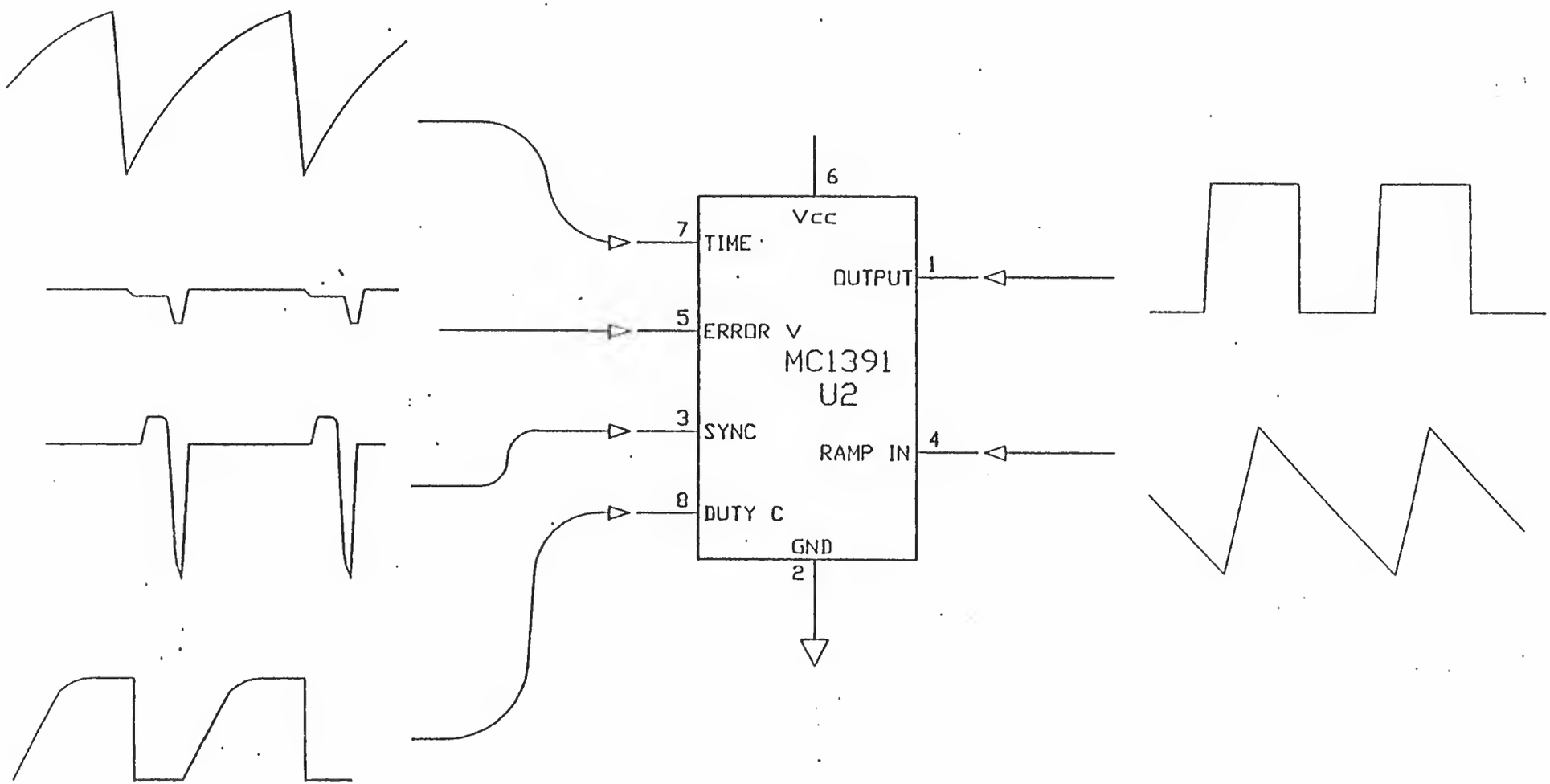
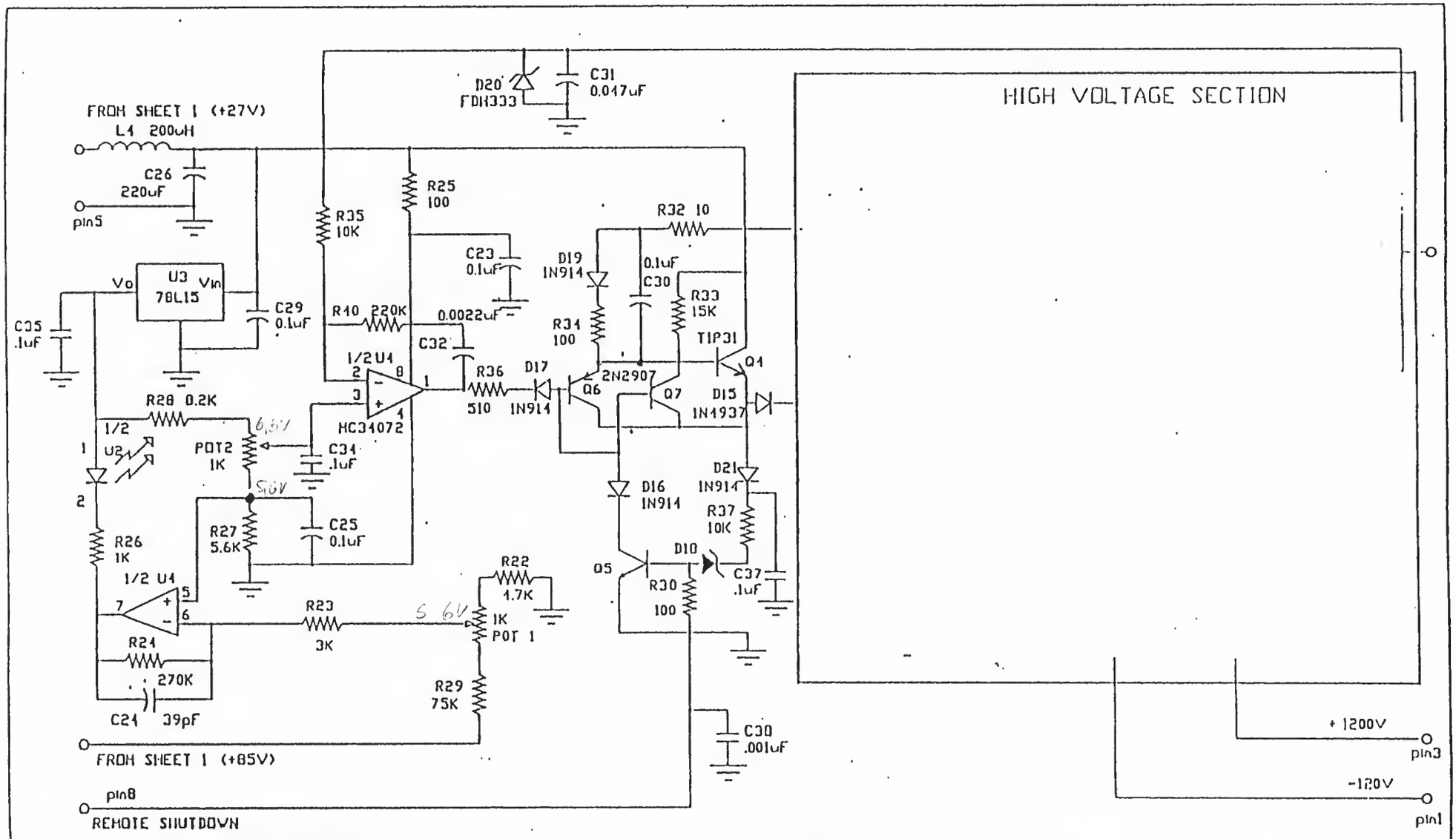

6
Vcc
7
TIME
OUTPUT
1
5
ERROR V
MC1391
U2
3
SYNC
RAMP IN
4
8
DUTY C
GND
2

FIGURE 1



WASATCH

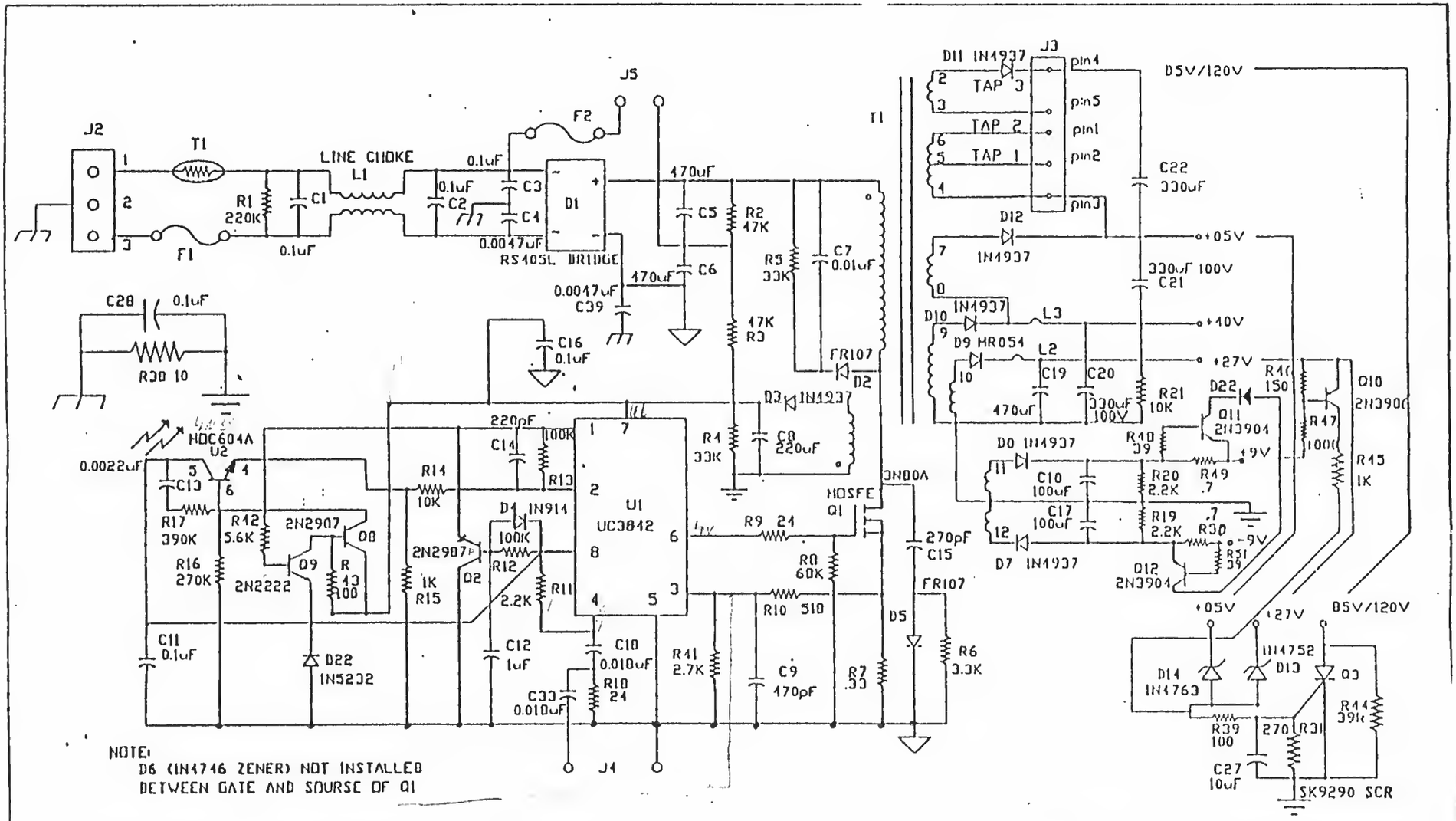
HIGH VOLTAGE

4100 SOUTH WEST TEMPLE
SALT LAKE CITY, UTAH 84107

TITLE: P65-02 POWER SUPPLY	MATERIAL:	SCALE: NONE	SHEET 2 OF 2
DRAWING #: VSCH-02A	FINISH:	DATE: 03-09-09	REVISION: A
	DRAWN BY: MINH TRAN	CHECKED BY:	

UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES AND DECIMALS
TOLERANCES ARE .XX ± 01 .XXX ± 005 ANGLES ± 1 DEG

P/N: Sigma-0965-00



WASATCH HIGH VOLTAGE 4100 SOUTH WEST TEMPLE SALT LAKE CITY, UTAH 84107	TITLE: P65-02 POWER SUPPLY DRAWING #: VSCS-02A	MATERIAL:	SCALE: NONE	SHEET 1 OF 2
		FINISH:	DATE: 03-09-09	REVISION A
		DRAWN BY: MINH TRAN	CHECKED BY:	
		UNLESS OTHERWISE SPECIFIED: DIMENSIONS ARE IN INCHES AND DECIMALS TOLERANCES ARE .XX ± 0.01, .XXX ± 0.005, ANGLES ± 1 DEG		

2N2222 → NPN/BC546
2N2907 → PNP/BC308

PN: 900-00006-00

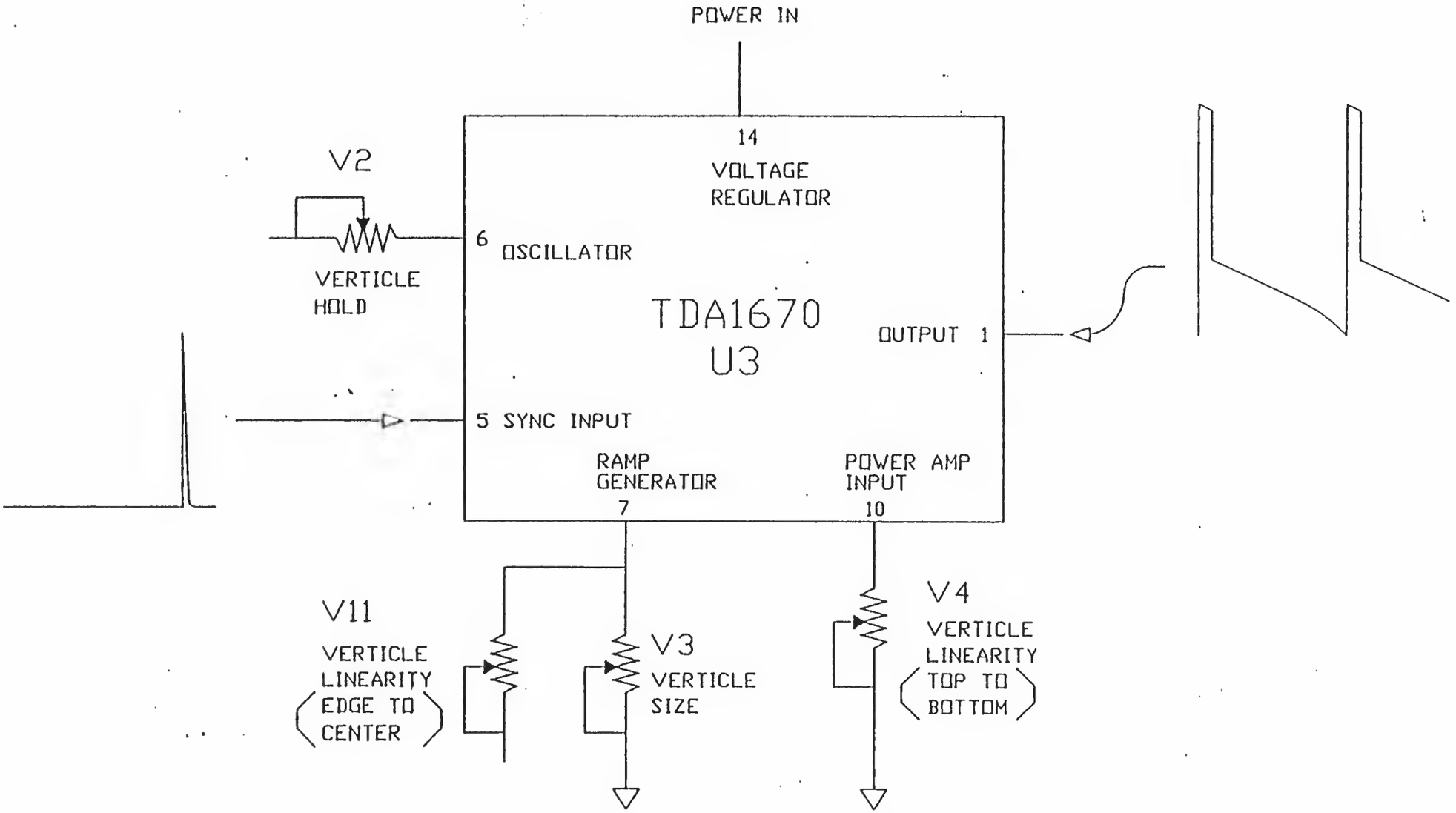
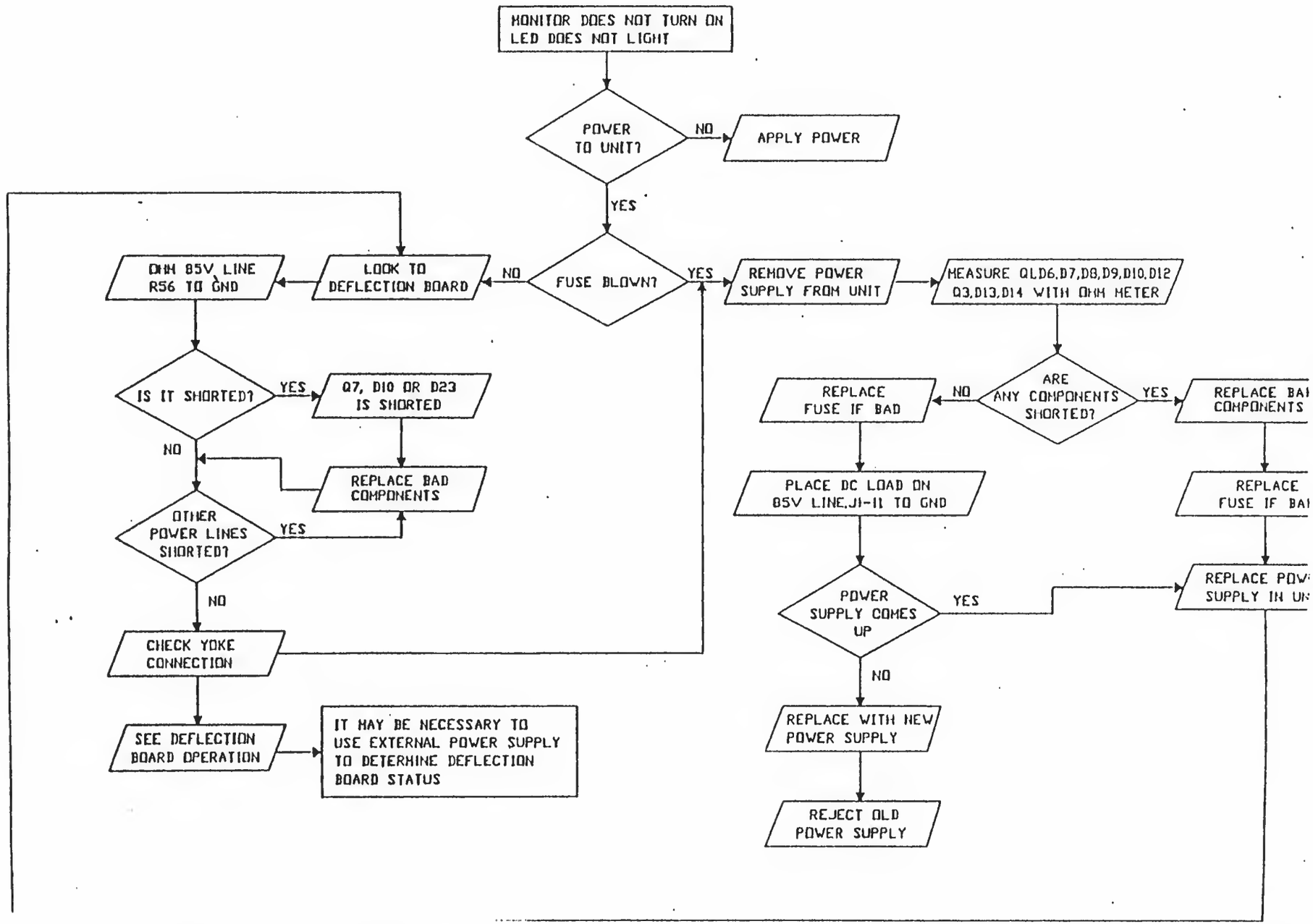
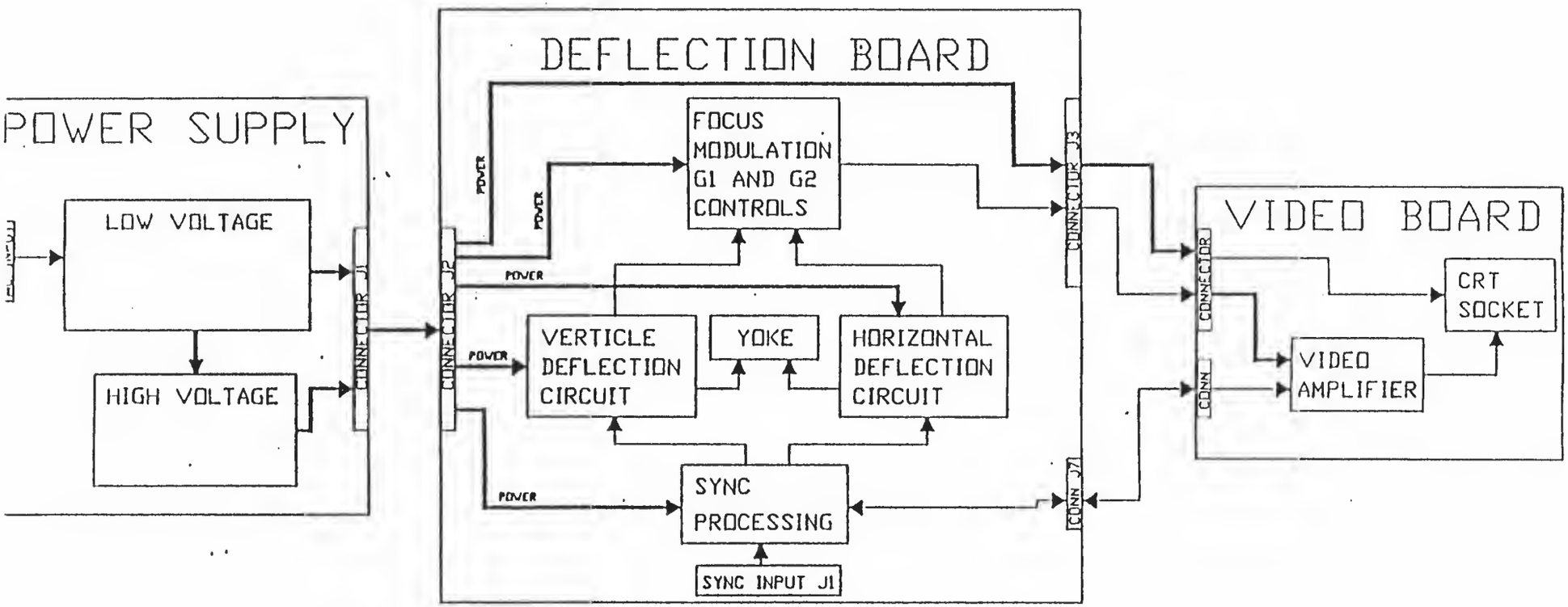

POWER IN
14
VOLTAGE
REGULATOR
V2
6 OSCILLATOR
VERTICLE
HOLD
TDA1670
U3
OUTPUT 1
5 SYNC INPUT
RAMP
GENERATOR
7
POWER AMP
INPUT
10
V11
VERTICLE
LINEARITY
EDGE TO
CENTER
V3
VERTICLE
SIZE
V4
VERTICLE
LINEARITY
TOP TO
BOTTOM

FIGURE 2


MONITOR DOES NOT TURN ON
LED DOES NOT LIGHT
POWER TO UNIT?
NO
APPLY POWER
YES
FUSE BLOWN?
NO
YES
LOOK TO DEFLECTION BOARD
OHM 85V LINE R56 TO GND
REMOVE POWER SUPPLY FROM UNIT
MEASURE QLD6,D7,D8,D9,D10,D12 Q3,D13,D14 WITH OHM METER
IS IT SHORTED?
YES
Q7, D10 OR D23 IS SHORTED
NO
REPLACE BAD COMPONENTS
OTHER POWER LINES SHORTED?
YES
NO
CHECK YOKE CONNECTION
SEE DEFLECTION BOARD OPERATION
IT MAY BE NECESSARY TO USE EXTERNAL POWER SUPPLY TO DETERMINE DEFLECTION BOARD STATUS
ARE ANY COMPONENTS SHORTED?
NO
YES
REPLACE FUSE IF BAD
REPLACE BAI COMPONENTS
PLACE DC LOAD ON 85V LINE,J1-11 TO GND
REPLACE FUSE IF BAI
POWER SUPPLY COMES UP
YES
REPLACE POW SUPPLY IN UN
NO
REPLACE WITH NEW POWER SUPPLY
REJECT OLD POWER SUPPLY


POWER SUPPLY
LOW VOLTAGE
HIGH VOLTAGE
CONNECTOR J1
DEFLECTION BOARD
CONNECTOR J2
POWER
POWER
POWER
POWER
POWER
FOCUS
MODULATION
G1 AND G2
CONTROLS
VERTICLE
DEFLECTION
CIRCUIT
YOKE
HORIZONTAL
DEFLECTION
CIRCUIT
SYNC
PROCESSING
SYNC INPUT J1
CONNECTOR J3
CONN J7
VIDEO BOARD
CONNECTOR
CONN
CRT
SOCKET
VIDEO
AMPLIFIER

MONITERM CORPORATION

Configuration and Alignment Specification

Customer Viking VCX 91DPI 220V Part Number 903-0279-03 Rev. B

Procedure	Paragraph	Parameter Limits
High Pot Test	38.2	Maximum Leakage Current 11mA
Burn-In	37.1	Use 1/2 Amp 9 Volt DC Load
Visual Inspection	4.1	Phillips 72µH, SPS Tap 2-5
Preliminary Setup	5.2	ECL video, Viking Cable with LED
Monitor Setup	5.4	Lowline = 198 VAC; Nominal = 220 VAC
Display Orientation	34.1	LMLS•UL
High Voltage	6.1	18,000 VDC; ±100 VDC
Page Size	7.4	82.0V ±1.0V, 14.0" x 10.50" ±0.10"
Page Centering In Raster	8.6	Dead Center
Video Centering	8.7	Mechanical Center
Vertical Linearity	9.5	5% Maximum
Horizontal Linearity	10.5	10% Maximum
Pincushioning	18.4	Screen Facing Magnetic North
Vertical Hold	23.3	
I ıote Brightness	11.2	Leave Remote For Max. Intensity
Highline/Lowline	12.1	265/198 VAC 60Hz
Intermittence	17.1	
Phase Locked Loop Drift	13.3	0.10" Maximum
Switching Power Supply	20.6	Tap 2-5
Brightness	14.5	G2= 650 VDC, ±30 Footlamberts ±3fL
Display Quality	16.1	Use Reference Display
Focus	15.6	Reference Q1002, Paragraph 9
Horizontal Retrace	27.1	Height 615V; Time 2.6 ±0.1µsec (REF)
Spot Kill	19.1	
AC Power Cycling	36.1	5 Cycles Minimum
120 Volt Operation	26.10	90/135 VAC 60 Hz
Adhesives	24.0	
Wrap-Up	32.1	Are you proud of this monitor?
Auxiliary Power Check	47.1	-9 VDC on pin 5 of 9D

Special Instructions

ıal alignment must be done on Moniterm 91 DPI controller card.

Quantum Generator Settings

Timing:		Horizontal:		Vertical:	
Dot Rate	62.176 MHz	Dots/Character	9	Lines/Character	16
Horizontal Rate	66.43 KHz	Total	104	Total	1000
Vertical Rate	66.43 Hz	Characters	80	Rows	60
		Drive Delay	78	Drive Delay	60
Step	2	Drive Width	4	Drive Width	3

All OP Codes Are Zero Except: OP 3.1, OP 7.1, OP 12.2, OP 14.1, OP 16.3
OP 4.1, OP 8.1, OP 13.3, OP 15.2,

Set Moniterm video generator outputs to: Video: +, Reverse Bit 3: Off Bit 2: Off Bit 1: On
H/C. Sync: H. sync H Sync: - V sync: -

AIAKI

Postbus 70, 4130 EB Vianen - Holland
Telefoon 03473 - 77272
Telefax 77200 - Telex 76409

Moniterm training, 19 april 1989

De training werd gegeven door: Dennis Pederson (international sales)
Rich Rheault (technical support)

De moniterm monitor bestaat uit:
- Switching power supply (SPS)
- High Voltage Power supply
- Deflection board
- Video board

SPS

- unieke 110/220 protection, bij 220V op 110 blaas je een zekering op, waardoor de voeding automatisch op 220V werkt.
- levert 9, 25, 40 Volt

High Voltage Power supply

- levert 120 en 1200 Volt

Deflection board

Zorgt voor sync en dus voor de complete beeldbesturing.

- unieke bescherming tegen inbranden bij vert./hor. defecten, schakelt dan de hoogspanning uit.

Video board

Verwerkt video signalen, tevens protectie tegen kortsluiting in Anode-buis. (door zwevende metaaldeeltjes en transport kan dit ontstaan, opbranden van deeltjes geen bezwaar > geeft typisch geluid).

MONITERM CORPORATION

Configuration and Alignment Specification

Customer Viking VCX 91DPI 220V Part Number 903-0279-03 Rev. B

Procedure	Paragraph	Parameter Limits
High Pot Test	38.2	Maximum Leakage Current 11mA
Burn-In	37.1	Use 1/2 Amp 9 Volt DC Load
Visual Inspection	4.1	Phillips 72µH, SPS Tap 2-5
Preliminary Setup	5.2	ECL video, Viking Cable with LED
Monitor Setup	5.4	Lowline = 198 VAC; Nominal = 220 VAC
Display Orientation	34.1	LMLS•UL
High Voltage	6.1	18,000 VDC; ±100 VDC
Page Size	7.4	82.0V ±1.0V, 14.0" x 10.50" ±0.10"
Page Centering In Raster	8.6	Dead Center
Video Centering	8.7	Mechanical Center
Vertical Linearity	9.5	5% Maximum
Horizontal Linearity	10.5	10% Maximum
Pincushioning	18.4	Screen Facing Magnetic North
Vertical Hold	23.3	
I ıote Brightness	11.2	Leave Remote For Max. Intensity
Highline/Lowline	12.1	265/198 VAC 60Hz
Intermittence	17.1	
Phase Locked Loop Drift	13.3	0.10" Maximum
Switching Power Supply	20.6	Tap 2-5
Brightness	14.5	G2= 650 VDC, ±30 Footlamberts ±3fL
Display Quality	16.1	Use Reference Display
Focus	15.6	Reference Q1002, Paragraph 9
Horizontal Retrace	27.1	Height 615V; Time 2.6 ±0.1µsec (REF)
Spot Kill	19.1	
AC Power Cycling	36.1	5 Cycles Minimum
120 Volt Operation	26.10	90/135 VAC 60 Hz
Adhesives	24.0	
Wrap-Up	32.1	Are you proud of this monitor?
Auxiliary Power Check	47.1	-9 VDC on pin 5 of 9D

Special Instructions

ıal alignment must be done on Moniterm 91 DPI controller card.

Quantum Generator Settings

Timing:		Horizontal:		Vertical:	
Dot Rate	62.176 MHz	Dots/Character	9	Lines/Character	16
Horizontal Rate	66.43 KHz	Total	104	Total	1000
Vertical Rate	66.43 Hz	Characters	80	Rows	60
		Drive Delay	78	Drive Delay	60
Step	2	Drive Width	4	Drive Width	3

All OP Codes Are Zero Except: OP 3.1, OP 4.1, OP 7.1, OP 8.1, OP 12.2, OP 13.3, OP 14.1, OP 15.2, OP 16.3

Set Moniterm video generator outputs to: Video: +, Reverse; H./C. Sync: H. sync; Bit 3: Off; H Sync: -; Bit 2: Off; V sync: -; Bit 1: On

AIAKI

Postbus 70, 4130 EB Vianen - Holland
Telefoon 03473 - 77272
Telefax 77200 - Telex 76409

Reparatie tips

Output	normale weerstand	check
9 V	4.3 M (zonder video board) 20 (met video board)	SPS, D8, R220
25 V	2 K	U2, U3, diodes rondom, SPS diodes
40 V	3-4 M	SPS D10
100 V	7.3 M	Q7, T2
120 V	14 M	High voltage box, deflection protection
1200 V	8-9 M	High voltage box, deflection protection, Q5, D5

SPS defecten > check V1, FET, transformator en output diodes
vervang ook V1 + FET bij transformator defect!!

> potmeter 1 regelt alle DC output levels
potmeter 2 regelt high voltage circuit

Defect spoelhuis > check T2, Q7, D32/37, al deze componenten vervangen, als je het spoelhuis vervangt!!

9 volt defect? evt. V5 op deflection board

AIAKI

Postbus 70, 4130 EB Vianen - Holland
Telefoon 03473 - 77272
Telefax 77200 - Telex 76409

Moniterm kent/kende 3 "Viking" modellen:

Viking 1	VXP 1000 electronica, metalen kast
Viking 2	VXP 1000 electronica, plastic kast
Viking 3	VCX 1000 electronica, plastic kast

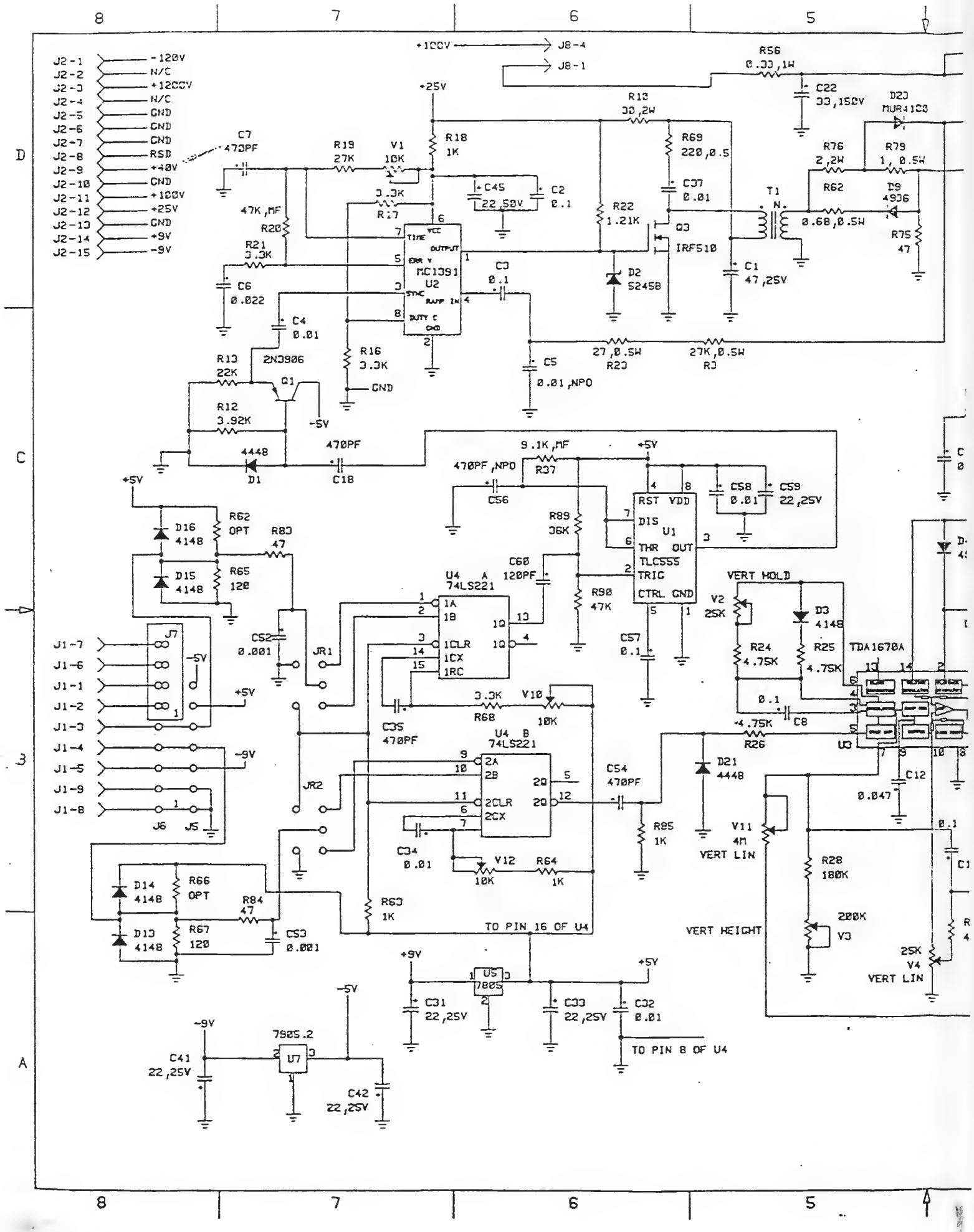
De VCX heeft een betere focus en een verbeterde voeding (beeld-storing). Deflection board is veel beter.

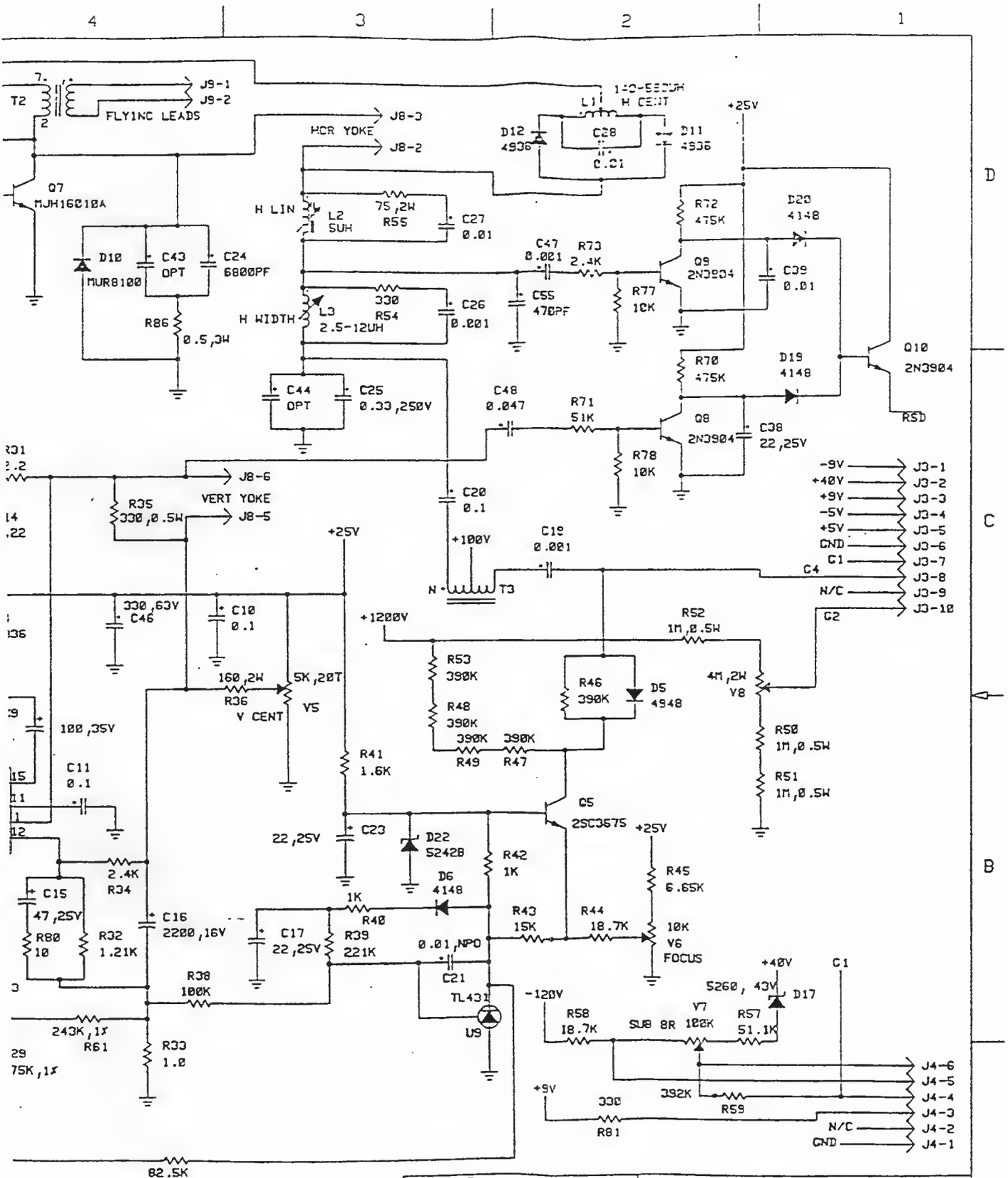
Atari krijgt VCX 1000.

Moniterm beschikt over een support BBS.

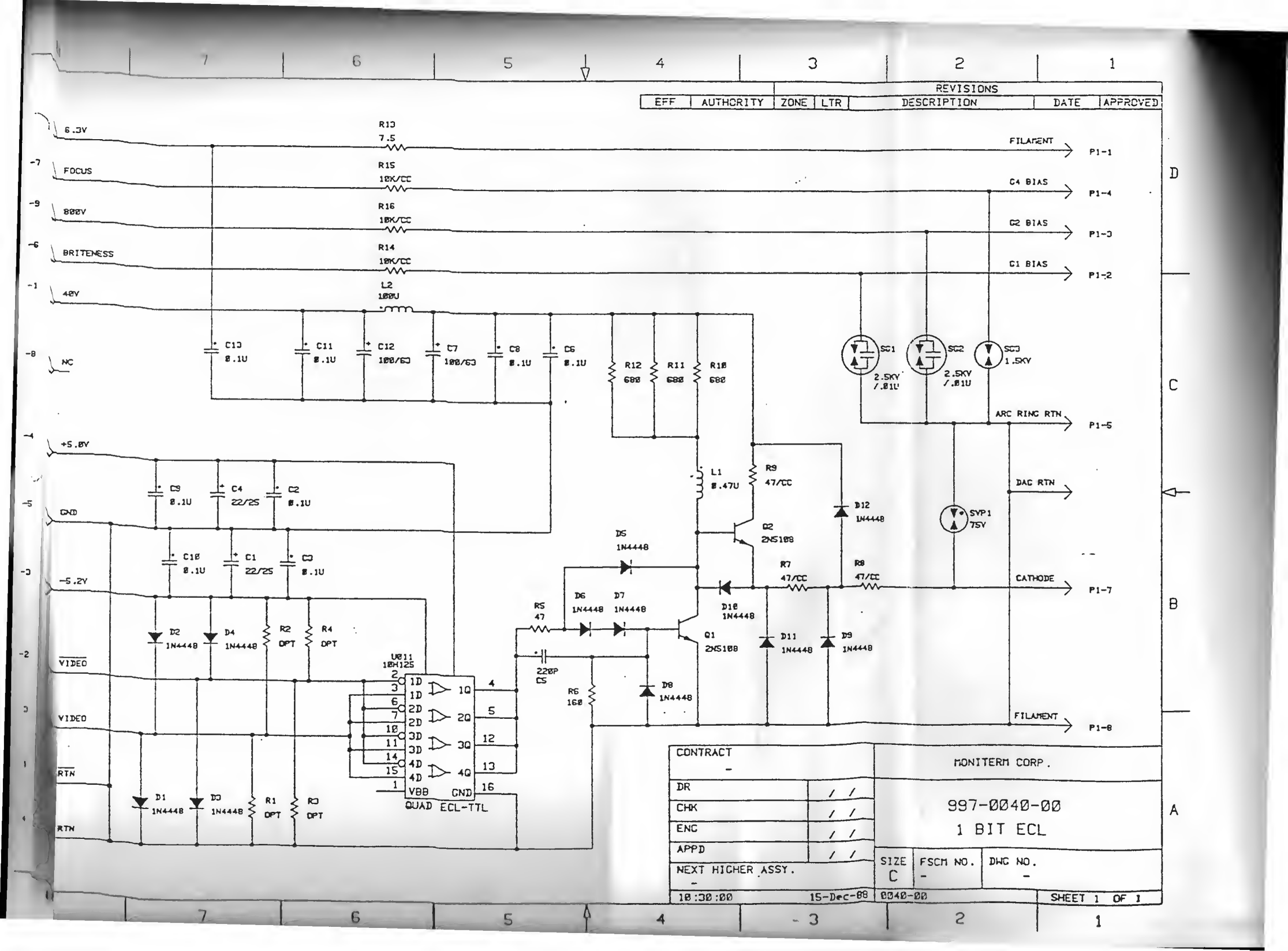
De Atari interface kaart is ontwikkeld door een extreme ontwikkelaar. De software is geschreven door deze ontwikkelaar en Ken Bradertcher van Atari Corp. Deze software werkt momenteel uitsluitend onder TOS 1.4 (geen 32K video memory beperking).De software kent geen mogelijkheid om te switchen tussen SM194 en SM124.

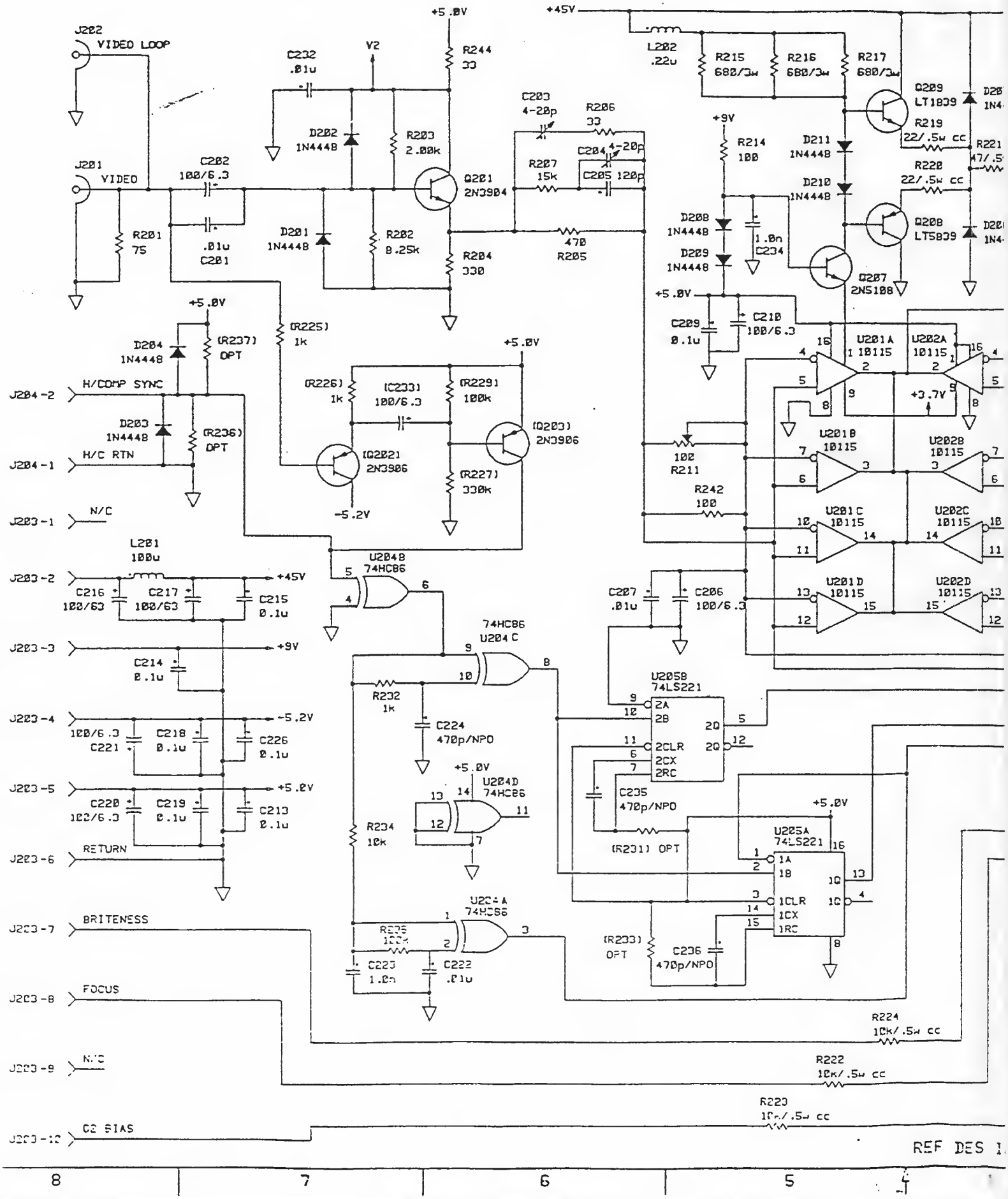
Wilfred Kilwinger

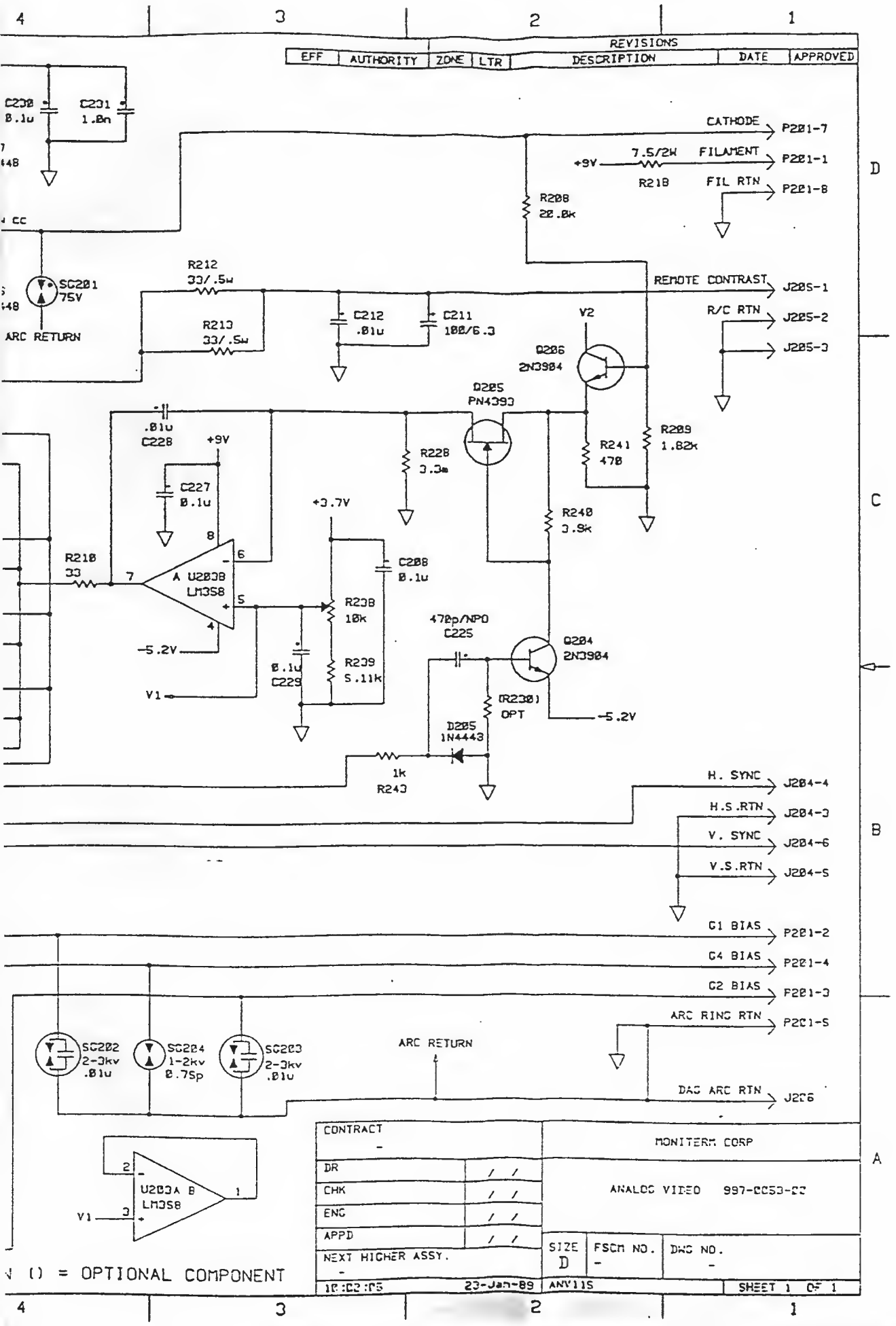

J2-1 -120V
J2-2 N/C
J2-3 +120CV
J2-4 N/C
J2-5 GND
J2-6 GND
J2-7 GND
J2-8 RSD
J2-9 +40V
J2-10 GND
J2-11 +100V
J2-12 +25V
J2-13 GND
J2-14 +9V
J2-15 -9V
+100V
J8-4
J8-1
+25V
R56 0.33,1W
C22 33,150V
D23 MUR4103
R13 33,2W
R69 220,0.5
R76 2,2W
R79 1, 0.5W
C7 470PF
R19 27K
V1 10K
R18 1K
C45 22,50V
C2 0.1
R17 3.3K
R20 47K,MF
R21 3.3K
C37 0.01
T1
R62
D9 4936
0.68,0.5W
R75 47
R22 1.21K
Q3 IRF510
C1 47,25V
MC1391 U2
C3 0.1
D2 5245B
C6 0.022
C4 0.01
R16 3.3K
GND
R13 22K
2N3906 Q1
R12 3.92K
-5V
27,0.5W R23
27K,0.5W R3
C5 0.01,NPO
4448 D1
470PF C18
9.1K,MF R37
470PF,NPO CS6
+5V
RST VDD U1
DIS
THR OUT
TLC555
TRIC
CTRL GND
CS8 0.01
CS9 22,25V
R89 36K
C60 120PF
R90 47K
CS7 0.1
D16 4148
R62 OPT
R83 47
D15 4148
R65 120
U4 A 74LS221
1A 1B 1CLR 1CX 1RC 1Q 2Q
CS2 0.001
JR1
J7
J1-7 J1-6 J1-1 J1-2 J1-3 J1-4 J1-5 J1-9 J1-8
J6 J5
VERT HOLD
V2 25K
D3 4148
R24 4.75K
R25 4.75K
TDA1670A
U3
0.1 C8
4.75K R26
C35 470PF
3.3K R68
V10 10K
U4 B 74LS221
2A 2B 2CLR 2CX 2Q
JR2
CS4 470PF
D21 4448
C12 0.047
R85 1K
V11 4M VERT LIN
C34 0.01
V12 10K
R64 1K
R63 1K
TO PIN 16 OF U4
D14 4148
R66 OPT
R84 47
D13 4148
R67 120
CS3 0.001
R28 180K
200K V3 VERT HEIGHT
25K V4 VERT LIN
U5 7805
C31 22,25V
C33 22,25V
C32 0.01
TO PIN 8 OF U4
-9V
7905.2 U7
C41 22,25V
C42 22,25V



CONTRACT -		MONITERM CORP	
DR	/ /	VCX DEFLECTION BOARD	
CHK	/ /		
ENG	/ /		
APPD	/ /		
NEXT HIGHER ASSY. -		SIZE D	FSCM NO. -	DWG NO. 991-0057-00
11:22:42	23-Jan-89 VCXDEFL	SHEET 1 OF 1	


REVISIONS
EFF | AUTHORITY | ZONE | LTR | DESCRIPTION | DATE | APPROVED
6.3V
FOCUS
800V
BRITENESS
40V
NC
+5.8V
GND
-5.2V
VIDEO
VIDEO
RTN
RTN
R13 7.5
R15 10K/CC
R16 10K/CC
R14 10K/CC
L2 100U
C13 0.1U
C11 0.1U
C12 100/63
C7 100/63
C8 0.1U
C6 0.1U
C9 0.1U
C4 22/25
C2 0.1U
C10 0.1U
C1 22/25
C3 0.1U
R12 680
R11 680
R10 680
L1 0.47U
R9 47/CC
R7 47/CC
R8 47/CC
R5 47
220P C5
R6 160
D2 1N4448
D4 1N4448
D1 1N4448
D3 1N4448
R2 OPT
R4 OPT
R1 OPT
R3 OPT
D5 1N4448
D6 1N4448
D7 1N4448
D8 1N4448
D10 1N4448
D11 1N4448
D9 1N4448
D12 1N4448
Q2 2N5108
Q1 2N5108
U811 10H125
QUAD ECL-TTL
SG1 2.5KV /.01U
SG2 2.5KV /.01U
SG3 1.5KV
SVP1 75V
FILAMENT P1-1
C4 BIAS P1-4
G2 BIAS P1-3
C1 BIAS P1-2
ARC RING RTN P1-5
DAC RTN
CATHODE P1-7
FILAMENT P1-8
CONTRACT -
DR / /
CHK / /
ENG / /
APPD / /
NEXT HIGHER ASSY. -
MONITERM CORP.
997-0040-00
1 BIT ECL
SIZE C
FSCM NO. -
DWG NO. -
10:30:00 15-Dec-88
0040-00
SHEET 1 OF 1


8
7
6
5
J202
VIDEO LOOP
J201
VIDEO
C232
.01u
V2
R244
33
+5.0V
+45V
L202
.22u
R215
680/3w
R216
680/3w
R217
680/3w
Q209
LT1839
R219
22/.5w cc
R221
47/.5
R220
22/.5w cc
Q208
LT5839
Q207
2N5188
D202
1N4448
R203
2.00k
C203
4-20p
R206
33
C204
4-20p
R207
15k
C205 120p
Q201
2N3904
C202
100/6.3
R201
75
.01u
C201
D201
1N4448
R202
8.25k
R204
330
470
R205
+9V
R214
100
D211
1N4448
D210
1N4448
D208
1N4448
D209
1N4448
1.0n
C234
+5.0V
C209
.01u
C210
100/6.3
U201A
1 10115
U202A
10115
+3.7V
U201B
10115
U202B
10115
100
R211
R242
100
U201C
10115
U202C
10115
U201D
10115
U202D
10115
C207
.01u
C206
100/6.3
+5.0V
D204
1N4448
(R237)
OPT
(R225)
1k
J204-2
H/COMP SYNC
D203
1N4448
(R236)
OPT
J204-1
H/C RTN
J203-1
N/C
(R226)
1k
(C233)
100/6.3
(R229)
100k
(Q202)
2N3906
(Q203)
2N3906
(R227)
330k
-5.2V
L201
100u
J203-2
C216
100/63
C217
100/63
C215
.1u
+45V
U204B
74HC86
J203-3
C214
.1u
+9V
74HC86
U204C
R232
1k
C224
470p/NPO
J203-4
100/6.3
C221
C218
.1u
C226
.1u
-5.2V
+5.0V
U204D
74HC86
J203-5
C220
100/6.3
C219
.1u
C213
.1u
+5.0V
R234
10k
J203-6
RETURN
U205B
74LS221
C235
470p/NPO
(R231) OPT
U205A
74LS221
U204A
74HC86
J203-7
BRITENESS
R235
100k
C223
1.0n
C222
.01u
(R233)
OPT
C236
470p/NPO
J203-8
FOCUS
R224
10k/.5w cc
J203-9
N/C
R222
10k/.5w cc
R223
10k/.5w cc
J203-10
G2 BIAS
REF DES I
8
7
6
5
4


REVISIONS
EFF | AUTHORITY | ZONE | LTR | DESCRIPTION | DATE | APPROVED
C230 .1u
C231 1.8n
CATHODE P201-7
+9V 7.5/2W FILAMENT P201-1
R218 FIL RTN P201-8
R208 22.8k
SC201 75V
ARC RETURN
R212 33/.5W
R213 33/.5W
C212 .01u
C211 100/6.3
REMOTE CONTRAST J205-1
R/C RTN J205-2
J205-3
V2
Q206 2N3904
Q205 PN4393
.01u C228
+9V
C227 .1u
R228 3.3k
R241 470
R209 1.82k
R240 3.9k
+3.7V
R210 33
A U203B LM358
C208 .1u
R238 10k
R239 5.11k
470p/NPO C225
Q204 2N3904
.1u C229
-5.2V
V1
(R230) OPT
D205 1N4443
1k R243
H. SYNC J204-4
H.S.RTN J204-3
V. SYNC J204-6
V.S.RTN J204-5
G1 BIAS P201-2
G4 BIAS P201-4
G2 BIAS P201-3
ARC RING RTN P201-5
SC202 2-3kv .01u
SC204 1-2kv 0.75p
SC203 2-3kv .01u
ARC RETURN
DAC ARC RTN J206
U203A B LM358
V1
() = OPTIONAL COMPONENT
CONTRACT -
DR / /
CHK / /
ENG / /
APPD / /
NEXT HIGHER ASSY. -
MONITERM CORP
ANALOG VIDEO 997-0053-02
SIZE D
FSCM NO. -
DWG NO. -
10:02:05 23-Jan-89 ANV11S
SHEET 1 OF 1